## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1947	((703/13) or (703/14) or (703/15)).CCLS.	USPAT; USOCR	OR	OFF	2008/07/08 09:01
S2	843	((713/167) or (713/194)).CCLS.	USPAT; USOCR	OR	OFF	2008/07/08 09:01
S3	665	(705/57).CCLS.	USPAT; USOCR	OR	OFF	2008/07/08 09:01
S4	1434	(716/1).CCLS.	USPAT; USOCR	OR	OFF	2008/07/08 09:02
S5	79	(S1 S2 S3 S4) and (obfuscat\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 09:02
S6	36	\$5 and (scrambl \$3 descrambl\$3 entangl\$3 detangl \$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 09:03
S7	35	S6 and (simulat \$4 model\$3 design\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 09:16
S8	5	S6 and (simulat \$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 09:16
S9	62	((simulat\$4 model \$3 design\$3) same (obfuscat \$4) same (circuit (IP adj core)))	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:19
S11	0	((scrambl\$4 and descrambl\$3) and (entangl\$3 and detangl\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:21

S12	6769	descrambl\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:21
S13	11	S9 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:22
S17	93	verilog hardware	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:35
S18	66	verilog hardware	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:36
S19	0	verilog hardware	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:37

S20	73	verilog hardware	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:39
S21	2	· \$ 1	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:39
S22	0	verilog hardware	USPAT; USOCR; EPO; JPO;	OR	ON	2008/07/08 10:40
S23	0	((intellectual adj property) IP\$core vhdl circuit hdl netlist) same (obfuscat\$4 and (entangl\$3 detangl\$3 scrambl \$3 descrambl\$3)) same (simulat\$4 model\$3 emulat \$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:44

	0	vhdl circuit hdl netlist circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:45
w.S25	3	((intellectual adj property) IP\$core vhdl circuit hdl netlist circuit) and (obfuscat\$4 and (entangl\$3 detangl\$3 scrambl \$3 descrambl\$3)) same (simulat\$4 model\$3 emulat \$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:45
S26	2182	(optimiz\$5 with IP)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:46
S28	0	scrambl\$3 and descrambl\$3 and entangl\$3 and detangl\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:48
S29	6768	(scrambl\$3 with descrambl\$3) (entangl\$3 with detangl\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:48
S30	7	S26 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:48
S31	21775	((IP\$core circuit) with simulation)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:50

S32	79	S29 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:50
S33	1132	(bain.inv.)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:54
S34	1	S33 and obfuscat \$4	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2008/07/08 10:55

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